WIDEBAND 3W AMPLIFIER EMPLOYING CLUSTER MATCHING

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ABSTRACT

High power, broadband monolithic amplifiers have inherent performance limitations and require specialized fabrication and design techniques to ensure optimal performance and high yield. The "cell cluster matching" design approach is presented as a solution to this power-bandwidth problem along with a detailed discussion of the high yield fabrication techniques used to implement it. In particular, a 3 W 8-12 GHz amplifier, employing the cluster matching technique, is discussed and some initial test results are presented.

INTRODUCTION

A fundamental concern to monolithic IC amplifier designers is determining the maximum power output-bandwidth product achievable consistent with acceptable yield and good performance. For the 3 W 8-12 GHz amplifier discussed herein (see Figure 1) the output stage requires a total gate periphery of 6400μm. With such a large FET, one in faced with several inherent performance limiting problems. First, if the 6400μm FET were composed of 32 directly combined 200μm cells, the low input impedance (1 to 2 ohms) and optimum output load impedance (5 to 6 ohms) would result in a difficult impedance transforming problem over a broad bandwidth (8-12 GHz) and substantial circuit losses. More importantly, in a FET this large, phase differences between the cells close to the center feed point and those farthest away from the feed point cause a significant reduction in FET gain and power output. This is particularly true at X-band frequencies and above. In addition, odd mode signals can be generated due to process variations inevitable across such a large FET structure. These odd modes contribute to further gain reduction and to the possibility of intercell oscillations. Careful circuit design considerations must be made to minimize these deleterious effects and maximize the power bandwidth product.

CELL CLUSTER MATCHING

An alternative to direct cell combining, as mentioned above, is to use a "cell cluster matching" design approach in conjunction with planar power combining techniques (see Figures 3 & 5). In this approach, the 200μm cells are grouped together into eight separate 800μm cell clusters. Note that matching is done at the 800μm cell cluster level where impedance levels are high. Each cell cluster is partially matched before combining, thereby resulting in an overall higher impedance level at the combining points and a corresponding improvement in performance over a broad bandwidth. Each cell cluster is first "double tuned" to a "convenient" resistive impedance level and combined with another partially matched cell cluster. A $\lambda/4$ transformer then transforms the combined resistive impedance level of each of the four cluster pairs to 200Ω. A "convenient" impedance level is defined as one which allows a practical line impedance to be used as the $\lambda/4$ transformer while not severely complicating the initial double tuning circuitry. The four cell cluster pairs, now transformed to 200Ω, are combined to produce the desired 50Ω match.

Note that since the cell cluster matching circuits are identical, the phase angles of the wavefronts reaching each cluster are identical thereby eliminating intercell phasing problems. Figure 2 shows an example of the impedance progression just described on the output or drain side of a single stage, 3 W amplifier using four 1600μm cell clusters. The intermediate impedance level in this design is 17Ω corresponding to a 59Ω $\lambda/4$ transformer.

By placing reistors, whose values are equal to the resistive impedance level looking into each partially matched cell cluster pair, at the ends of each $\lambda/4$ line and tying the other end of each resistor to a common node, a four-way Wilkinson power combiner/splitter is formed. This type of combiner has good isolation characteristics over reasonably broad bandwidths. Implanted resistors are used and are fabricated at the same time as the FET active channel. This isolation feature is used to eliminate odd mode oscillation tendencies and/or make the circuit tolerant to processing variations. Unfortunately, on a planar structure such as a monolithic amplifier, long inductive bondwires and airbridges must be used to connect the isolation resistors together. This inductance causes the isolation of the combiner to decrease with increasing frequency. To eliminate this effect, series capacitors have been added at the ends of the resistors (Figure 3) to resonate out the inductive effects at

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midband (10 GHz) and better approximate a short circuit. The isolation characteristics of this "resonant node" structure were calculated for the various port to port combinations. The isolation calculated is that seen by the FETs (i.e., FET capacitance and the initial matching circuitry are included). For the worst case (two outer ports) of the input and output combiners, isolations between 25 and 50 dB were obtained across the band.

AMPLIFIER FABRICATION TECHNIQUES

A direct selective ion implantation process is used at Westinghouse for fabricating power FETs and IC's and is routinely yielding power FETs with power outputs of 0.5 - 0.7 W/mm of gate periphery at 12 GHz. An outline of this fabrication procedure is given in the following paragraphs.

Material Growth

The gallium arsenide semi-insulating substrates used for the fabrication of monolithic integrated circuits are produced in-house from <100> oriented, single crystals grown by the liqud encapsulated Czochralski (LEC) technique using a Melbourn high-pressure puller (Metal Res. Ltd.). The crystals are pulled from the melt contained in a pyrolytic boron nitride (PBN) crucible following compounding in-situ; a liquid B_2O_3 encapsulant and inert gas over-pressure are employed to prevent As sublimation which would result in low resistance, nonstoichio metric crystals.

Careful elimination of electrically active impurities, paricularly Si which can be introduced by SiO_2 crucibles, eliminates the need to counter-dope with Cr to compensate residual shallow donors. These crystals exhibit state-of-the-art chemical purity and minimize residual impurity activation during processing. As grown, the material exhibits sheet resistivities (R_s) of $3x10^8 \Omega$/square and mobilities of 5000 cm^2/volt-sec.

Ion Implantation

Implantation processing originates with plasma deposition of a 900 Å Si_3N_4 primary encapsulation layer on the front surface. This layer remains on the surface through processing to prevent mechanical damage and/or chemical contamination as well as to prevent dissociation during the implant anneal. 2500 Å of phosphosilicate glass (PSG) deposited after the Si_3N_4 serves as both an implantation mask and a registration layer; the PSF layer remains on the wafer through the implant anneal and is plastic at the annealing temperature, thereby reducing stress.

Contact photolithography and ion milling are used to open windows to the PSG/Si_3N_4 interface for ion implantation. Implants are made at two different Si^{29} ion energies (260 KeV and 125 KeV) through the 900 Å thick Si_3N_4 at ambient temperature to provide a flat profile whose depth is $\approx$ 2750 Å.

After the stripping of the photoresist and the deposition of a second PSG layer the wafers are annealed through controlled cycle to 860°C for 15 minutes to activate the implant.

Metalization Technology

Following the implantation and activation of the Si^{29} implant, ohmic contacts for the sources and drains of the FETs are deposited by a liftoff process on to the gallium arsenide using the alignment marks ion milled into the surface during the ion implantation processing. The metal used for the ohmic contacts consists of 1100 Å gold 12% germanium alloy, 500 Å nickel and 400 Å of platinum. This metal system is alloyed at 490°C for 10 secs in an argon-10% hydrogen atmosphere and the contacts thus formed are very reproducible from run to run and across the 2" wafers with values of contact resistance less than $3x10^{-6} \Omega\text{-cm}^2$, monitored routinely using the TLM method.

The gates of the FETs are formed using contact lithography and masks made by E-beam on 4-inch, 90 mil thick quartz plates. Two photoresist systems have been employed. The first of these is AZ1350J photoresist in combination with near-UV (405 nM) radiation and has resulted in gates down to 0.7μm long. A chlorobenzene soak of the AZ1350J photoresist provides an overhang which greatly assists the liftoff of the gate metallization which consists of 500 Å titanium, 400 Å platinum and 6500 Å of gold. Dimensions down to 0.5μm have been achieved using a double layer structure of a co-polymer of polymethyl methacrylate (PMMA) and 25% methacrylic acid (MAA) on top of a lyer of PMMA and exposed by deep UV (210 nM) radiation.

Prior to deposition of the gate metals the gate region is wet chemically etched to a depth of 1000 Å to provide a recessed gate structure.

Following testing of the now gated transistors, the circuit metallization is defined using a thick layer of AZ1350J (3.7μm). The pattern places inductors on the surface of the gallium arsenide in the form of microstrip lines which are plated up to a thickness of 5μm later in the fabrication process when the air bridges are formed. In addition, the bottom plates of metal-insulator-metal (MIM) capacitors are defined together with the drain interconnections on the FETs.

The circuit metalization is 11500 Å of metal which is composed of chromium (500 Å), palladium (1000 Å) and gold (10000 Å). For the M-I-M capacitor circuit designs an additional layer of chromium (500 Å) is added to provide good adhesion of the insulating layer (sputtered silicon dioxide). The dielectric for the M-I-M capacitors is bias-sputtered SiO_2, 3000 Å thick, that is patterned by lift-off using 2.5μm of AZ1350J photoresist.

Interconnections of the sources of the FETs and the top plates of the MIM capacitors are formed by "air bridges" as shown in the scanning electron micrograph of Figure 6. The process consists of depositing a lower layer of AZ1375 photoresist (4μm thick), which is then opened to expose the areas to be connected by the bridge. 500 Å of titanium and 500 Å of gold are then evaporate over the whole wafer and a second layer of AZ1375 (4μm) is then used to define the bridge itself. The opened areas are plated up with gold to a thickness of 5μm, the top photoresist removed and the thin gold and titanium layers chemically etched away. Removal of the lower resist layer completes the process and results in high yield (> 99%) rugged interconnections.

The front of the wafer is now complete and the remaining steps are thinning of the slice, formation of vias and metalizations of the back of the wafer. The slice is thinned from 500μm down to 100μm to provide the correct spacing between the microstrip lines on the front of the wafer and the ground plane on the back. Thinning is accomplished by a combination of lapping in a semi-automatic jig and a final chem-mechanical polishing. A rough surface finish of the back of the wafer has been shown to have a deleterious effect on circuit losses.

Air bridges and via holes are used, respectively, to interconnect the FET source pads and to provide low inductance source grounds. The via holes also improve circuit layout flexibility by permitting grounding of circuit elements interior to the chip.

Vias are formed by wet chemical etching using a slightly preferential etch to produce coneshaped holes through the 100μm substrate. The vias and the back of the wafer are then coated with Cr-Au-Ni-Au metalization, the nickel acting as a barrier to the gold-tin alloy used to bond the finished chips to the microwave test carrier.

The slice is then sawed into chips and those chips which have acceptable DC FET and passive characteristics are mounted and bonded onto RF carriers for testing.

3 W 8-12 GHz SINGLE STAGE AND FOUR STAGE AMPLIFIERS

The cell cluster matching technique has been used to design a 3 W, 8-12 GHz single stage amplifier in addition to the aforementioned four stage amplifier. The first iteration of this 6400μm FET single stage amplifier (Figure 3) produced 2.58 Watts (cw) out at 8 GHz with$\approx$5 dB associated gain and a 1 dB bandwidth of 1.56 GHz (Figure 4). As far as is known, this is the highest reported output power for an X-band monolithic amplifier.

The complete four stage amplifier has also been fabricated (Figure 5) and is now in the process of evaluation. The complexity of this chip is best illustrated by its parts count; i.e., 60 cells (total gate width 12 mm), 30 vias, 39 overlay capacitors, and 140 air bridges, as well as its overall size which is 6.9 mm x 5.3 mm. In spite of this complexity, DC yield on the first run is 12 chips out of 100. RF results will be presented at the conference.

CONCLUSIONS

The cell cluster matching technique was described as a solution to the three main problems associated with large periphery power FET amplifiers. Namely, the problems of: 1) matching to low impedance levels over broad bandwidths, 2) ensuring equal power and phase to each FET cell, and 3) minimizing inter-cell interactions through the use of the "resonant node" isolation structure.

High yield fabrication techniques were also discussed. In particular, direct selective ion implantation into high purity LEC grown semi-insulating substrates was discussed as a key fabrication technology.

Finally, a 3 W, 8-12 GHz four stage and single stage amplifier were discussed as an implementation of the cell cluster matching and fabrication techniques. An initial result of 2.58 W at 8 GHz with 5 dB gain was obtained from the single stage amplifier.

ACKNOWLEDGEMENTS

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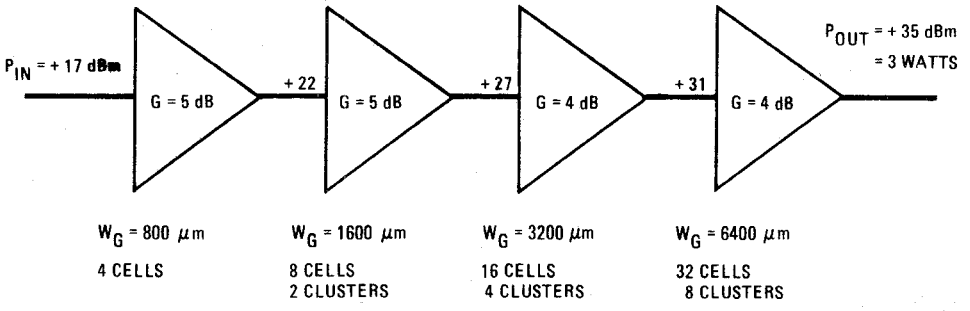

Figure 1. Block diagram of a four stage, 3 W, 8-12 GHz amplifier.

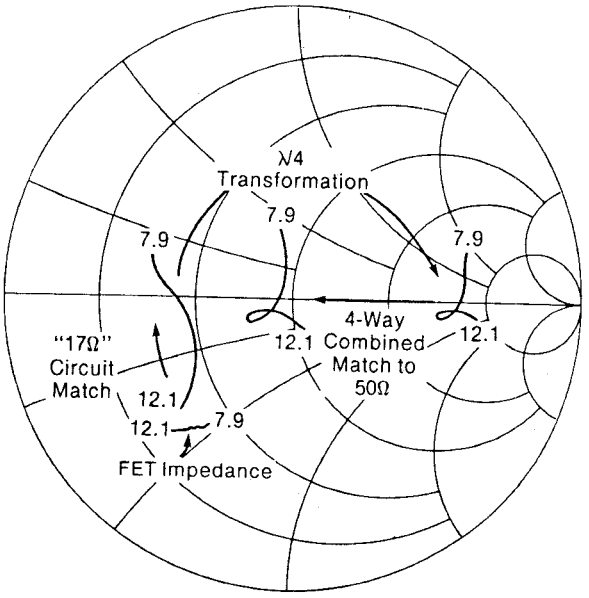

Figure 2. Impedance progression for a cell cluster matched, 3 W single stage amplifier design using four 1600 μm cell clusters.

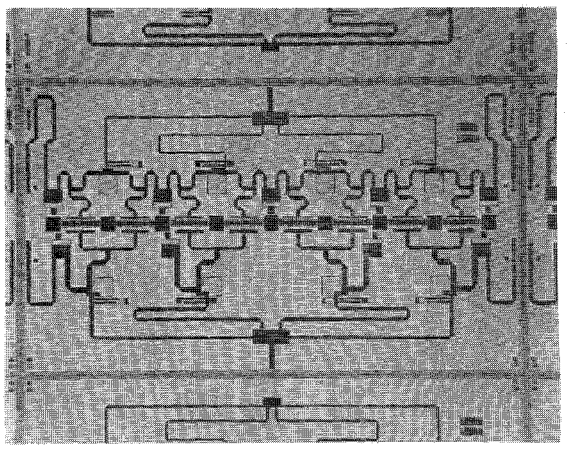

Figure 3. 8-12 GHz, 3 W single stage amplifier. Eight 800 μm cell clusters are used.

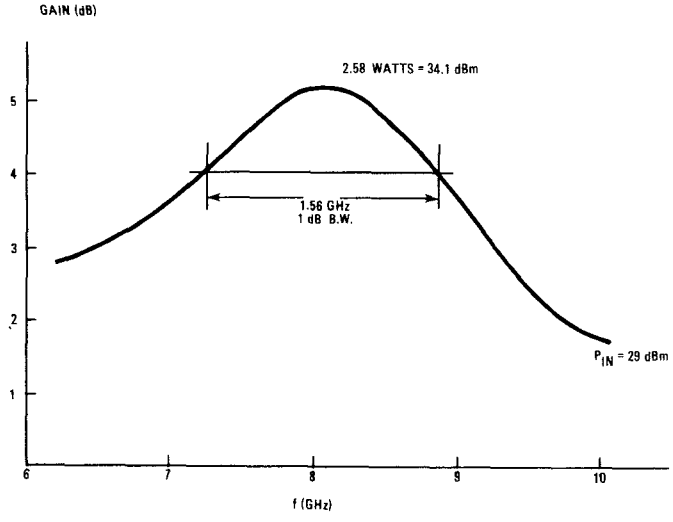

Figure 4. Measured gain vs. frequency plot for the amplifier in Figure 3.

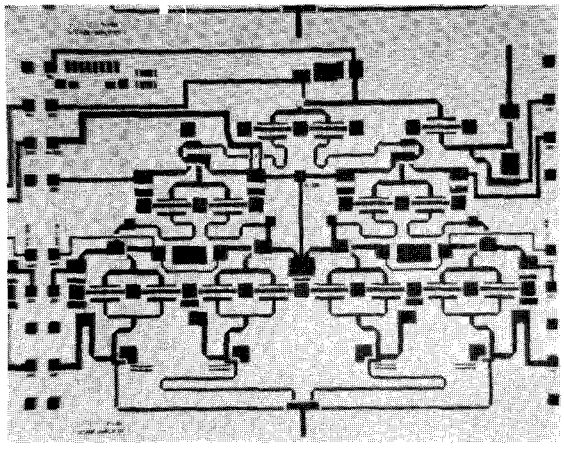

Figure 5. 8-12 GHz, 3 W four stage amplifier.

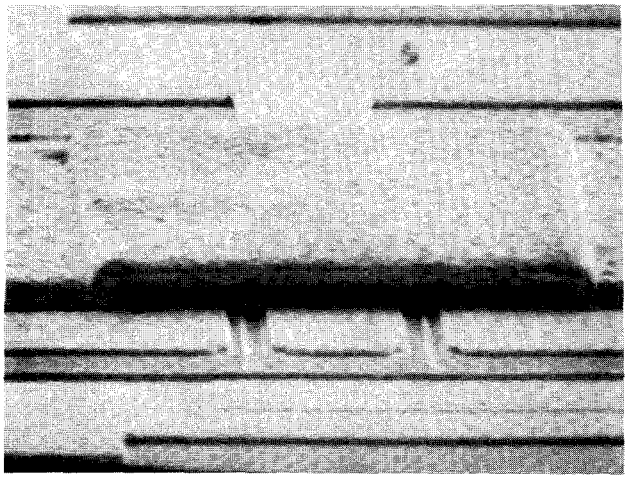

Figure 6. Air bridge interconnection on a GaAs monolithic circuit (5 μm high, 6 μm thick and 100 μm long).